R20 Regulation *Subject code: 3P4EB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, June 2026

COMPUTER ORGANIZATION AND ARCHITECTURE
(CSE)

Maximum Marks: 70 Date: 10.06.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Define Computer Organization.	2M	1	L1
2	List any four memory reference instructions.	2M	1	L1
3	List any four Bit manipulation instructions of 8086.	2M	2	L1
4	What is meant by instruction?	2M	2	L1
5	Why do we use dividend alignment while performing division operation of binary numbers?	2M	3	L1
6	What is IEEE standard for Binary Floating-point numbers?	2M	3	L1
7	Write the formula for the average access time experienced by the processor in a system with two levels of caches.	2M	4	L1
8	What do you mean by memory mapped I/O?	2M	4	L1
9	How the time slice method works?	2M	5	L1
10	Define Processor Synchronization.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	a) Explain the data transfer between register and memory. b) Explain shift micro-operations with an example.	5M 5M	1	L2
	OR			
12	Explain the execution of a complete instruction with an example.	10M	1	L2
13	a) Explain the control sequence required for branch instruction. b) Write simple Assembly language program and identify all the segments.	5M 5M	2	L2
	OR			
14	Explain the significance of Flag register and describe all flags with respect to 8086 Microprocessor.	10M	2	L2
15	a) Write about Arithmetic and Logic Unit with neat diagram. b) Explain Integer representation.	5M 5M	3	L2
	OR			

16	Explain Floating point arithmetic for Addition and Subtraction with example.	10M	3	L2
17	Explain Virtual memory in detail.	10M	4	L2
	OR			
18	a) Discuss the DMA driven data transfer techniques. b) Explain the basic concepts memory system.	5M 5M	4	L2
19	a) Explain the inter – processor communication using message passing and shared variable. b) Draw and explain centralized shared memory architecture.	5M 5M	5	L2
	OR			
20	a) Explain the Vector Processing in detail. b) Write about Array processing.	5M 5M	5	L2